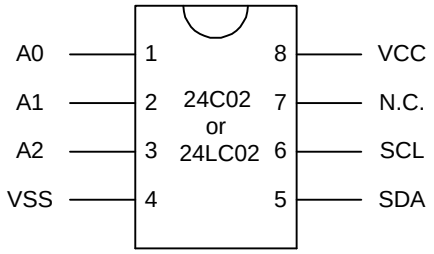
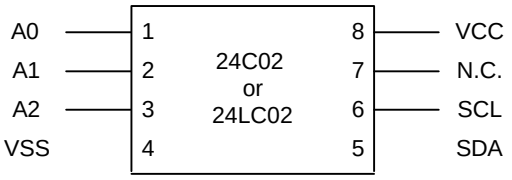
FEATURES

- ✧ State –of –the-Art Archiecture
- ✧ Non-volatile data storage
- ✧ Standard Voltage and Low Voltage Operation
- ✧ 5.0(Vcc=4.5V to 5.5V) for CP24C02
- ✧ 3.0(Vcc=2.7V to 5.5V) for CP24LC02
- ✧ ESD Protection
- ✧ Low standby current
- ✧ Page Write Buffer
- ✧ Self-timed write cycle(including auto-erase)
- ✧ Minimum of 100,000 write/erase cycle per word
- ✧ 10 years data retention after 100K write/erase cycle
- ✧ Unlimited read cycles
- ✧ Durable and Reliable
- ✧ 2 wire I^2C serial interface

CONNECTION DIAGRAM



Dual-In-Line package



TSSOP

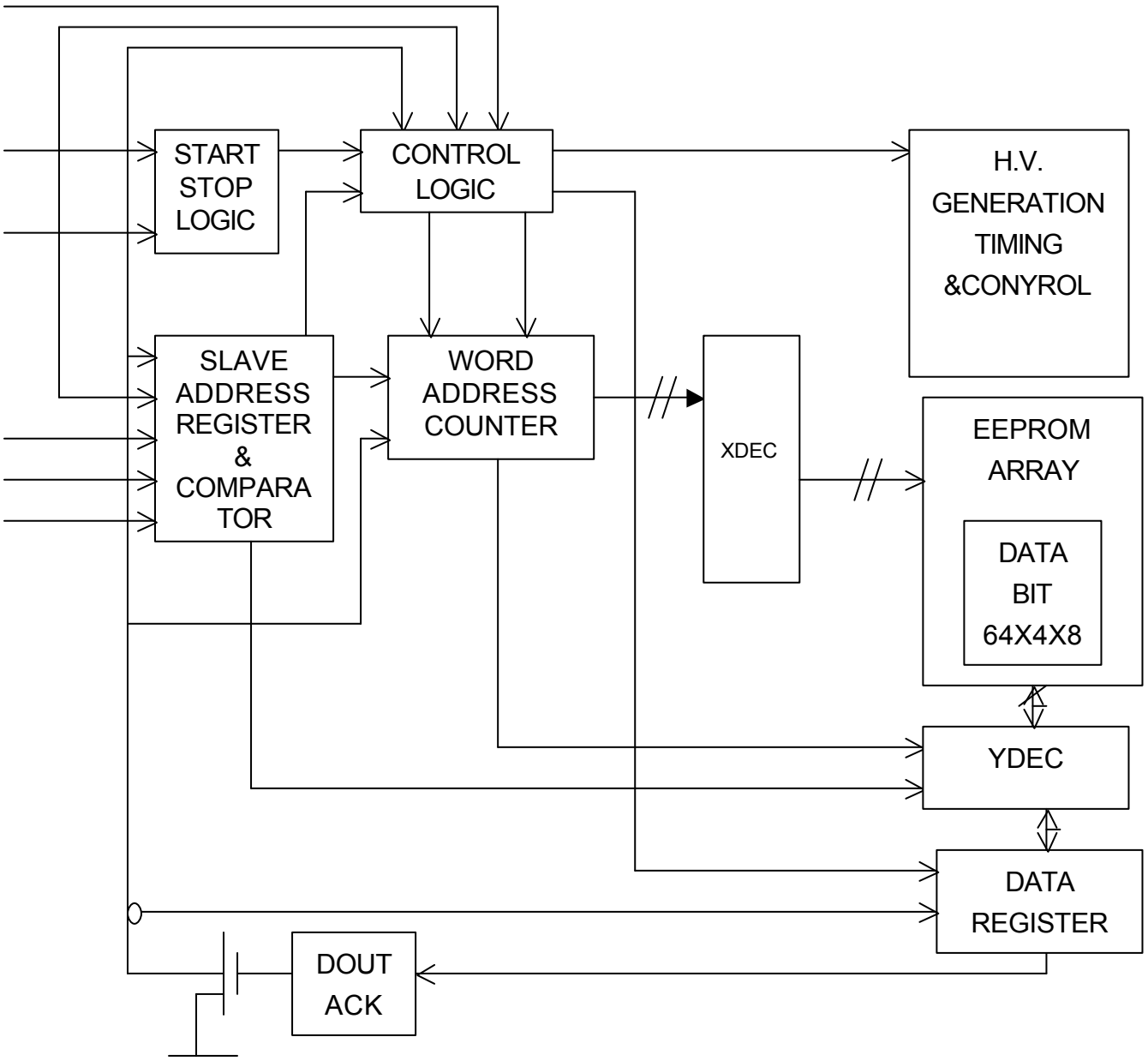
GENERAL DESCRIPTION

The 24C02/24LC02 is low cost,non-volatile,2048-bit serial EEPROM with enhanced security device and conforms to all specifications in the I^2C 2 wire protocol and is designed to minimize device pin count and simplify PC board layout requirements.The upper half of the memory then disabled (Write Protected) by connecting the WP pin to $V_{CC.}$ This section of memory then becomes unalterable unless WP is switched to V_{SS}. The 24C02/24LC02's communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microcomputer) and the slave EEPROM devices(s). In addition, the bus structure allows for a maximum of 16K of EEPROM devices(s). This is supported by the family in 2K, 4K, 8K, 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROM (not to exceed 16K).

CERAMATE EEPROM are designed and tested for application requiring high endurance, high reliability, and low power consumption.

This datasheet contains new product information. CERAMATE TECHNICAL CO., LTD. reserves the right to modify the product specification without notice. NO liability assumed as a result of the use of this product. NO right under any patent accompany the sale of the product.

BLOCK DIAGRAM



PIN DESCRIPTIONS

SERIAL CLOCK

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a bi-direction pin used to transfer data or security into and out of the device. It is an open drain output and may be wire-O red with any number of open drain or open collector output. Thus, the SDA bus requires a pull-up resistor to Vcc (typical 4.7KΩ for 100KHZ, 1KΩ for 400KHZ)

DEVICE ADSRESS INPUTS (A0, A1, A2)

Device address pin A0, A1, A3 are connected to Vcc or Vss to configure the EEPROM address

The following table (Table A) shows the active pins across the 24L/LCXX DEVICE family

TABLE A

Device	A0	A1	A2
24C02/24LC02	ADR	ADR	ADR
24C04/24LC04	XP	ADR	ADR
24C08/24LC08	XP	XP	ADR
24C016/24LC016	XP	XP	XP

ADR indicates the device address pin.

XP indicates that device address pin don' t care but refers to an internal PAGE BLOCK MAMORY segment.

WRITE PROTECTION (WP)

If WP connected to Vcc, PROGRAM operation onto the whole memory will not be executed. READ operation are possible. If WP connected to Vss, normal memory operation is enabled, READ/WRITE over the entire memory is possible.

FUNCTIONAL DESCRIPTION

APPLICATIONS

CERAMATE' s electrically erasable programmable read only memories (EEPROMs) offer valuable security features including write protect function, two write modes, three read modes, and a wide variety memory size. Typical applications for the I^2C bus and 24XC0XX memories are included in SANS (small-area-networks), stereos, televisions, automobiles and other scaled-down systems that don' t require tremendous speeds but instead cost efficiency and design simplicity.

ENDURANCE AND DATA RETENTION

The 24C02/24LC02 is designed for applications requiring up to 100,000 programming cycles (byte write and page write). It provides 40 years of secure data retention, without power after the execution of 100,000 programming cycles.

DEVICE OPERATION.

The 24C02/24LC02 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the 24C02/24LC02 is considered a slave in all applications.

Clock and data Conventions

Data states on the SDA line can change only during SCL LOW.SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. (Shown in Figure 1 and 2)

Start Condition

A HIGH to LOW TRANSITION OF THE SDA line while the clock (SCL) IS HIGH DETERMINES A START condition. All commands must be preceded by a START condition. (Shown in Figure 2)

Stop Condition

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a stop condition. (Show in Figure2)

Acknowledge

Each receiving device, When addressed is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit. The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition (Shown in figure 4)

Device Address

After generation a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24C02W/24LC02W, 3-bit device address (A02A1 A0) and a 1-bit value indication the read or write mode. All I2C EPROM's use and internal protocol that defines a PAGE BLOCK size of 2K bits. The eighth bit of slave address determines if the master device wants to read or write to the 24C02W/24LC02W. (Refer to table B)

The 24C02/24LC02 monitors the bus for it's corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Table B

Operation	Control Code	Chip Select	R/W
Read	1010	A2 A1 A0	1
Write	1010	A2 A1 A0	0

A2 A1 A0 are used to access device address for 24C02W/24LC02W, 2K bit's size device.

WRITE OPERATIONS

Byte Write

Following the start signal from the master, the master transmitter places the slave address onto the bus. This indicates to the address slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle

Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C02/24LC02.After After receiving another acknowledge signal from the 24C02/24LC02 the master device will transmit the data word to be written into the address memory location. The 24C02/24LC02 acknowledge written into the addressed memory location. The 24C02/24lc02 acknowledges again and the master generates a stop condition. This period the 24C02/24LC02 will not generate acknowledge signal. (Shown in Figure 4)

Acknowledge polling

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be imitated immediately. This involves the master sending a start condition followed by the control byte for a write command(R/W=0). If the device is still busy with the write cycle. Then no ACK will return. If the cycle is complete then the device will return the ACK and the master can then proceed with the next read or write commands.

Write PROTECTION

Programming the upper half of the memory will not take place if the WP pin of the 24C02/24LC02 is connected to Vcc the 24C02/24lc02 will accept slave and byte address, but if the memory accessed is write protected by the WP pin, the24C02/24LC02 will not generate an acknowledge after the first byte of data has been received, and thus programming cycle will not be started when the stop condition is asserted.

Each programming operation (BYTE WRITE for data) must satisfy two conditions before users initiate self-timed programming cycle. The first is that Vcc value must exceed a lock-out value which can be ad dusted by Analog Tevhnology, Inc.The second is that the upper half the memory is unoroted by connection WP to Vss.

READ OPERATION

Read operation are initiated in the same way as write operations with thaw exception that the R/W bit of the slave address is set to one. There are three basic types of read operation: current address read, and sequential read.

Current Address Read

The 24C02/24LC02 contains an address counter that maintains the address of the last accessed word, internally incremented by one. Therefore if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n+1 upon receipt of the slave address with R/W bit set to one, the 24C02/24LC02 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C02/24LC02 discontinues transmission (Shown in Figure 5)

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must set. Sending the word address to 24C02/24LC02 as part of a write operation does this. After the word address is sent the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with R/W bit set to a one. The 24C02/24LC02 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC02/24LC02 discontinues transmission. (Shown in Figure 6)

Sequential Read

Sequential read is initiated in the same way as a random read except that after the 24C02/24LC02 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24C02/24LC02 to transmit the next sequentially addressed 8-bit word (Shown in Figure 7). To provide sequentially read the 24C02/24LC02 contains an internal address pointer, which is incremented by one at the completion of each operation. This address pointer allows the entire Page Block (2K bits) memory contents to be serially read during one operation.

Noise Protection

The 24C02/24LC02 employs a Vcc threshold circuit, which disables the internal erase/write logic if the Vccc is below 1.5 volts at normal conditions. The SCL and SDA inputs have filter circuits, which suppress noise spikes to assure proper device operation even on a noisy bus.

ABSOLUTE MAXIMUM RATNGS

Storage Temperature……..-65^{o}C to 125^{o}C

Voltage with Respect to Ground…….-0.3 to +6.5V

NOTE: These are STRESS rating only. Appropriate conditions for operating these devices given elsewhere may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

OPERATION CONDITIONS

Temperature under bias: 24C02/24LC02…….0^{o}C to +70^{o}C

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS
(Vcc=5V+/-10%, 24C02/24LC02;Vcc=3V+/-10%, 24LC02)

Symbol	Parameter	Conditions	24C02W/ 24LC02W		24LC02W		Units
			Min	Max	Min	Max	
Icc1	Operating Current (Program)	SCL=100KHZ CMOS Input Levels	-	10	-	8	mA
Icc2	Operating Current (Read)	SCL=100KHZ CMOS Input Levels	-	1	-	1	MA
Isb	Standby Current	SCL=SDA=0V	-	1	-	1	UA
IIL	Input Leakage	Vin=0V to Vcc	-1	+1	-1	+1	UA
Vol	Output Leakage	Vout=0V to Vcc	-1	+1	-1	+1	UA
Iil	Input Low Voltage		-0.1	0.8	-0.1	0.15Vcc	V
V1h	Input High Voltage		2	Vcc+0.2	0.8Vcc	Vcc+0.2	V
Vol1	Output Low Voltage	Iol=2.1MA TTL	-	0.4	-	0.4	V
Voh1	Output High Voltage	Ioh=-400Ua TTL	2.4	-	2.4	-	V
Vol2	Output Low Voltage	Iol=10UA CMOS	-	0.2	-	0.2	V
Voh2	Output High Voltage	Ioh=-10UA CMOS	Vcc-0.2	-	Vcc-0.2	-	V
Vlk	Vcc Lockout Voltage	Programming Command Can Be Excuted	Default	-	Default	-	V

AWITCHING CHACTERISTICS (Under Operting Conditions)

AC ELECTRICAL CHARACTERISTICS
(Vcc=5V+/-10%, 24C02;Vcc=3V+/-10%, 24LC02)
(Vcc=5V+/-10%, 24C02 Fast Mode)

Parameter	Symbol	24C02W/24LC02W		24C02W(Fast Mode)		Units
		Min	Max	Min	Max	
Clock frequency	Fscl	0	100	-	400	KHZ
Clock high time	Thigh	4000	-	600	-	Ns
Clock low time	Tlow	4700	-	1200	-	Ns
SDA and SCL rise time	Tr	-	1000	-	300	Ns
SDA and SCL fall time	Tf	-	300	-	300	Ns
START condition hold time	Thd: Sta	4000	-	600	-	Ns
START condition setup time	Tsu:Sta	4700	-	600	-	Ns
Data input hold time	Thd: Dat	0	-	0	-	Ns
Data input setup time	Tsu:Dat	250	-	100	-	Ns
Stop condition setup time	Tsu:Sto	4000	-	600	-	Ns
Output valid from clock	Taa	300	3500	100	900	Ns
Bus free time	Tbuf	4700	-	1200	-	Ns
Input filter spike suppression (SDA and SCL pins)	Tsp	-	100	-	50	Ns
Data out hold time	Tdh	300	-	50	-	Ns
Write cycle time	Twr	-	10	-	10	ms

CAPACITANCE TA=25Oc,f=250KHZ

Symbol	Parameter	Max	Units
C_{out}	Output capacitance	5	PF
C_{in}	Input capacitance	5	PF

A.C. Condition of Test

Input Rise and Fall times	Vcc x0.1 to Vcc x0.9
Input Rise and Fall times	10ns
Input and Output Timming level	Vcc x 0.5
Output Load	1 TTL Gate and CL=100pf

Timing Diagram

FIGURE 1. Bus Timing

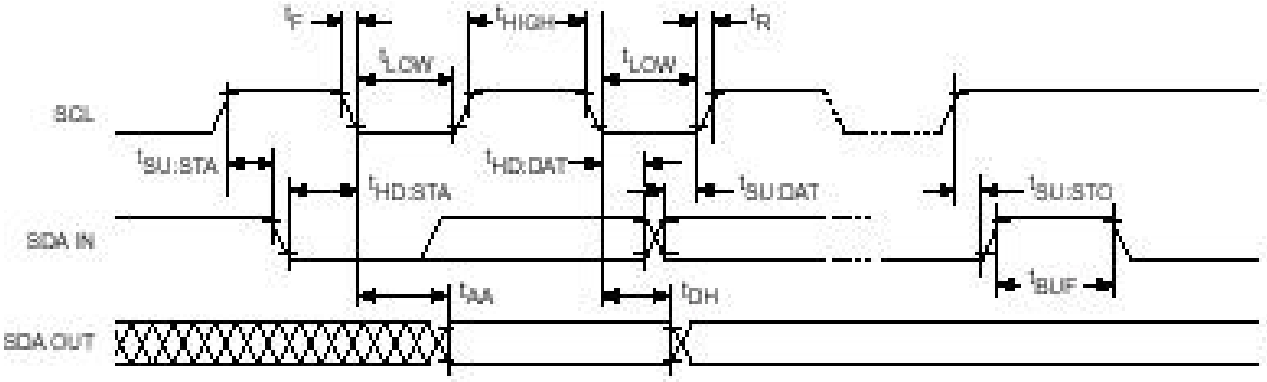


FIGURE 2. Start/Stop Timing

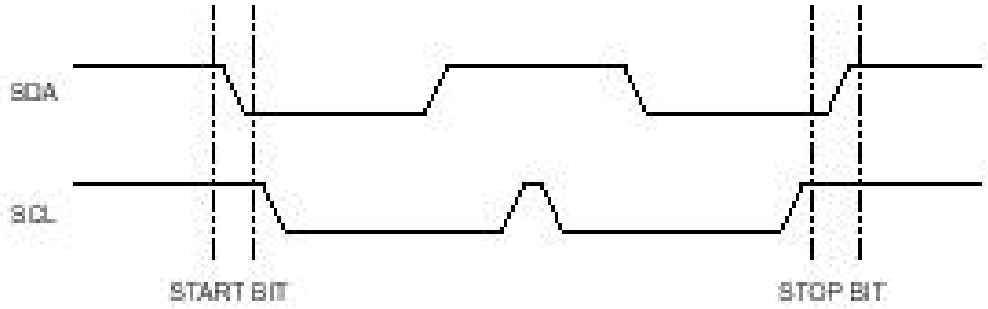


FIGURE 3. Acknowledge Response From Receiver

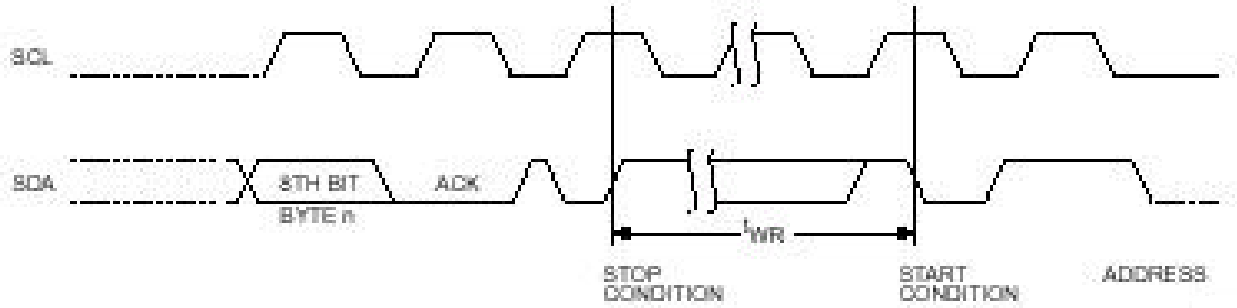


FIGURE 4 Write Cycle Timing

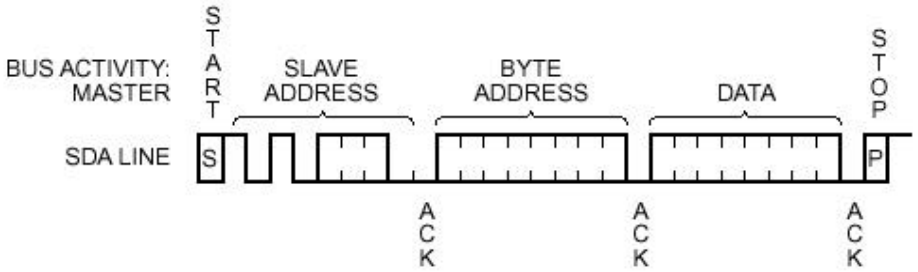


FIGURE-5 Slave Address Bits

24LC02	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**R/W**

FIGURE-6 Byte Write Timing

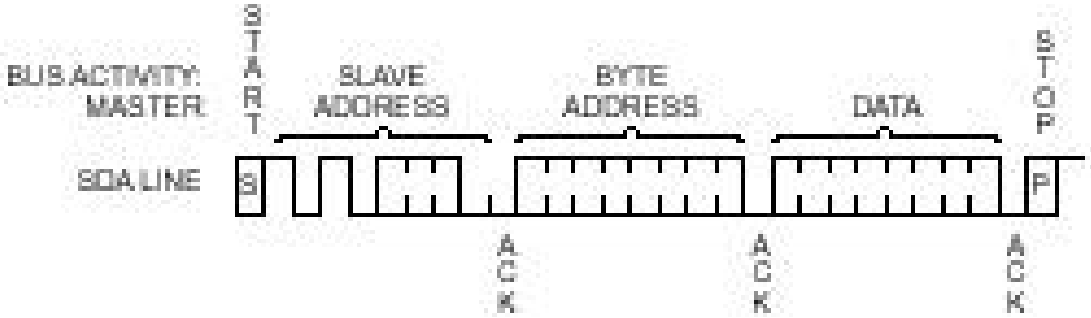


FIGURE 7 Page Write Timing

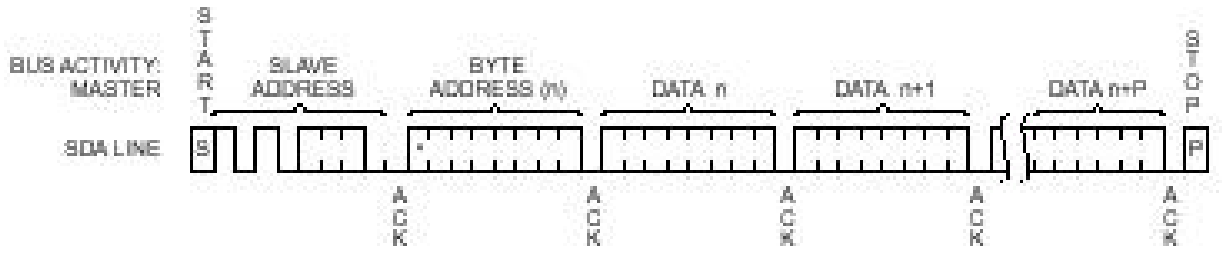


FIGURE 8 Immediate Address Read Timing

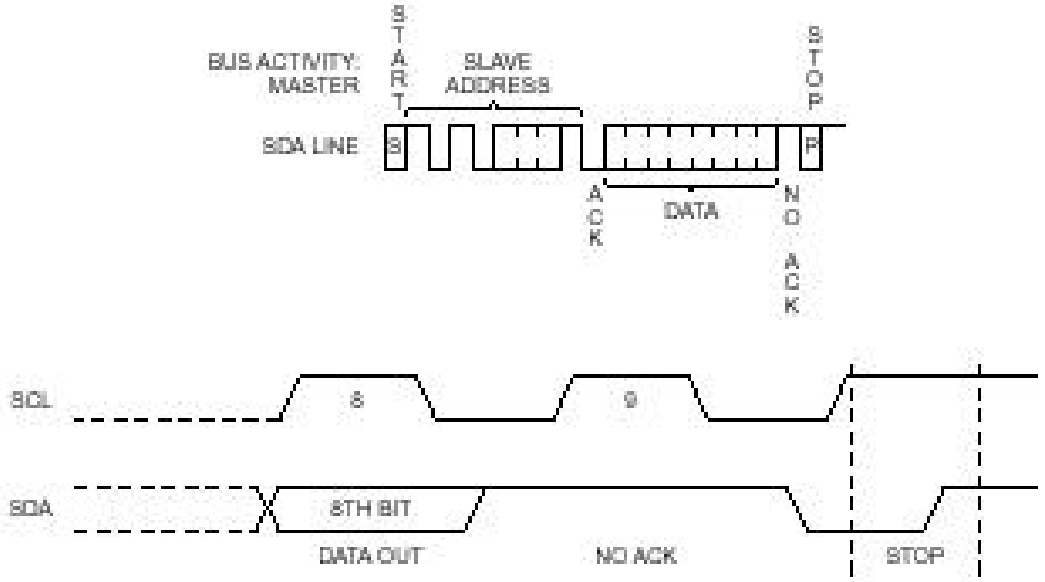


FIGURE 9 Selective Read Timing

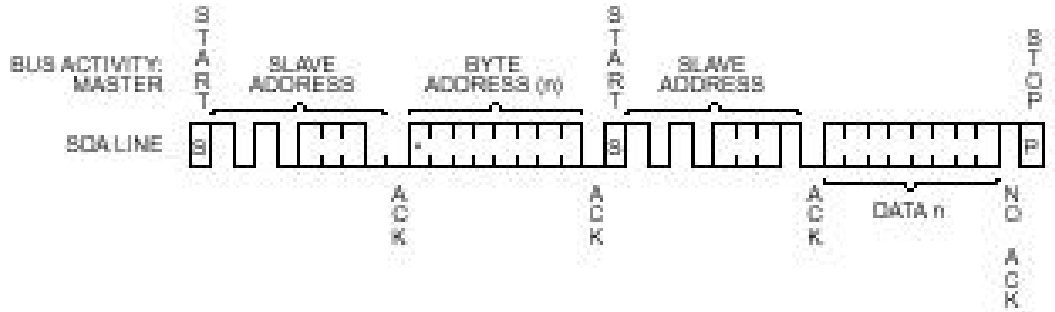
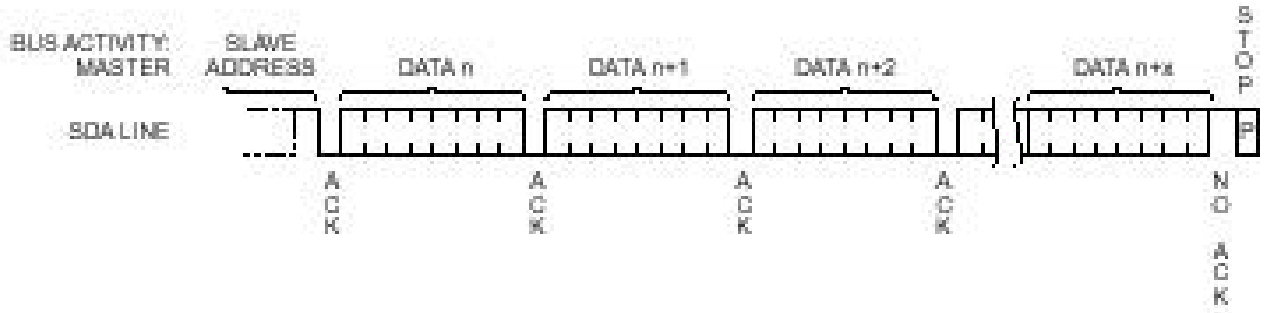
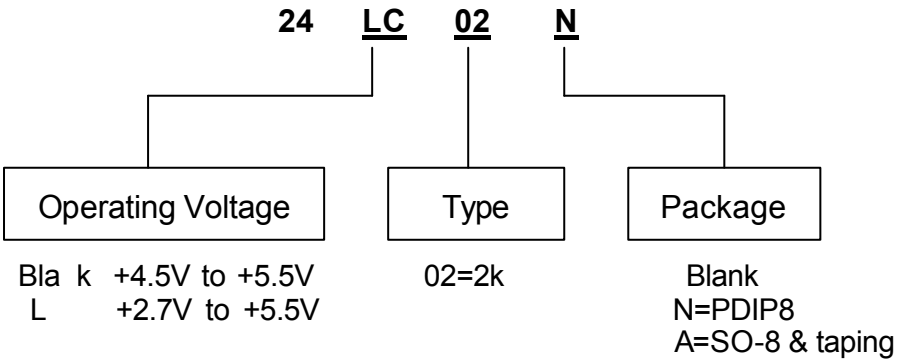


FIGURE 10 Sequential Read Timing

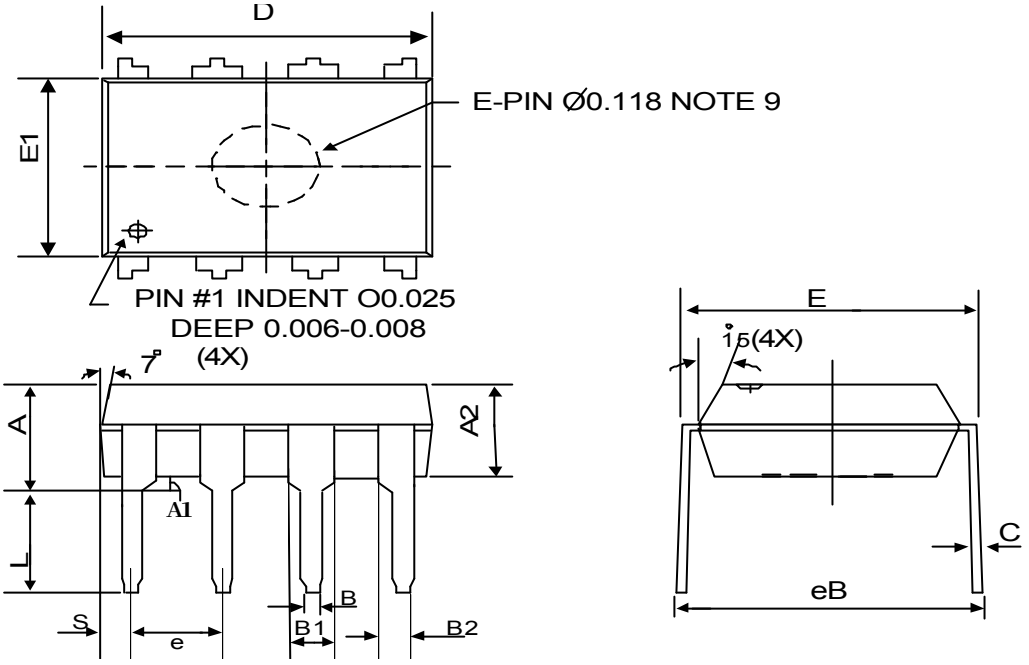


ORDERING INFORMATION



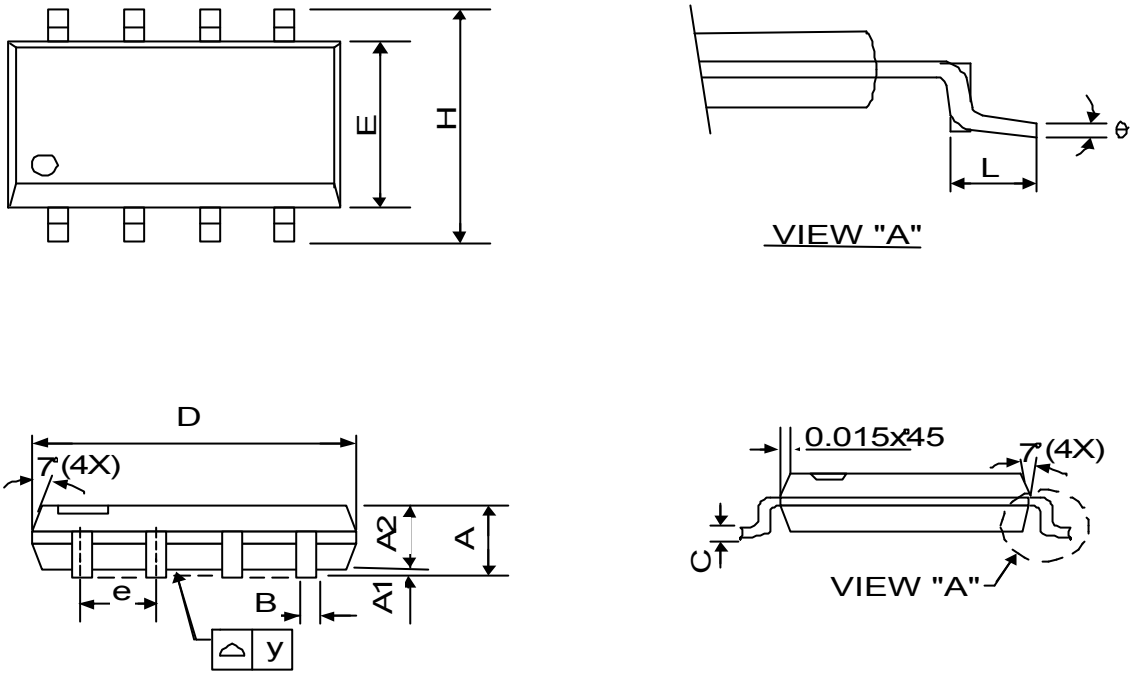
PACKAGE DIAGRAMS

Plastic Dual-in-line Package (PDIP)



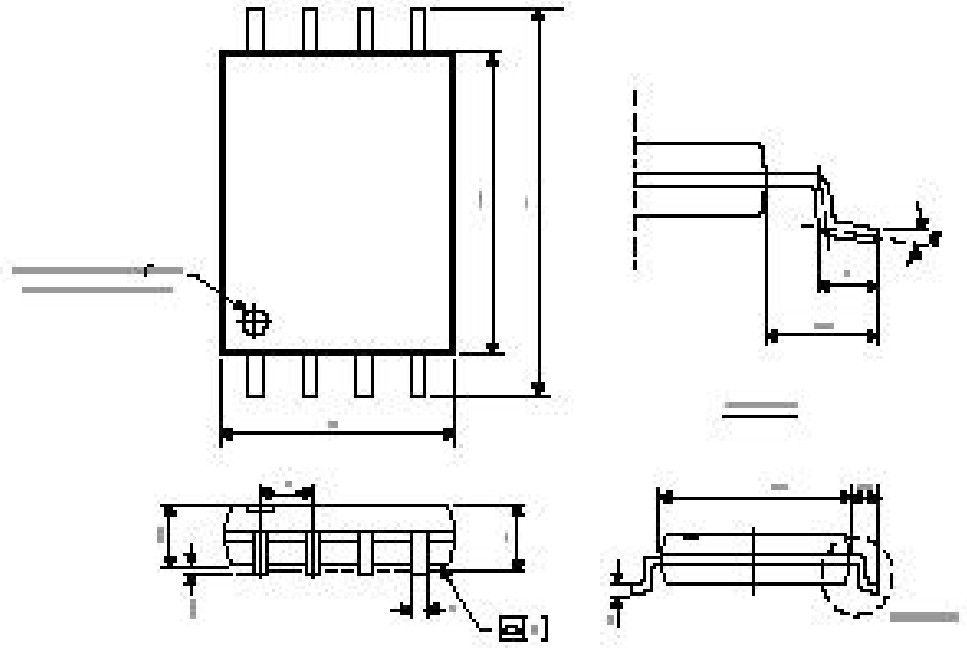
SYMBOL	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	5.33	-	-	0.210
A1	0.38	-	-	0.015	-	-
A2	3.25	3.30	3.45	0.128	0.130	0.136
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.14	1.27	1.52	0.045	0.050	0.060
B2	0.18	0.99	1.17	0.032	0.039	0.046
C	0.20	0.25	0.33	0.008	0.010	0.013
D	9.12	9.30	9.53	0.359	0.366	0.375
E	7.62	-	8.26	0.300	-	0.325
E1	6.20	6.35	6.60	0.244	0.250	0.260
e	-	2.54	-	-	0.100	-
L	3.18	-	-	0.125	-	-
Eb	8.38	-	9.40	0.330	-	0.370
s	0.71	0.84	0.97	0.028	0.033	0.038

JEDEC Small Outline Package (SO-8)



SYMBOL	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	-	0.25	0.004	-	0.010
A2	-	1.45	-	-	0.057	-
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	3.81	3.91	3.99	0.150	0.154	0.157
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
Y	-	-	0.10	-	-	0.004
θ	-0°	-	8°	0°	-	8°

8L TSSOP PACKAGE OUTLINE DRAWING



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	1.05	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.20	0.25	0.28
C	-	0.127	-
D	2.90	3.05	3.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
Y	-	-	0.10
θ	0^o	4^o	8^o